Wednesday, May 15th

Time	Paper Title
8:30 – 9:00	Registration
9:00 – 9:20	OPENING SESSION Panagiotis Dimitrakis Vassilios Ioannou Pascal Normand Christos Tsamis
9:20 – 10:05	***From 3D devices to 3D stacking, next challenges and perspectives*** ***Thomas Ernst***
10:05-10:25	Enhanced Threshold Voltage Tuning in SOI MOSFET with Ferro-BOX **Sorin Cristoloveanu**
10:25-10:45	Experimental Extraction of Self-Heating in SOI Nanowire MOSFETs at Cryogenic Temperatures **Marcelo Pavanello**
10:45 – 11:00	Coffee Break
11:00-11:20	Low-Loss Silicon Substrates with PN Passivation in 28 nm FD-SOI **Martin Rack**
11:20-11:40	Comparison of Self Heating Effect between SOI and SOSiC MOSFETs **Huiping Zhu**
11:40-12:00	Thermal-coupling characterization of FD-SOI FETs at cryogenic temperatures **Martin Vanbrabant**
12:00-12:20	Enhancing Cryogenic Performance of FDSOI Logic Circuits Using Back Biasing and Threshold Voltage Engineering **Tapas Dutta**
12:20-12:40	High-Endurance Bulk CMOS One-Transistor Cryo-Memory **Curt A. Richter**
12:40-13:00	Analysis of Electron Mobility in 7-Level Stacked Nanosheet GAA nMOSFETs **Michelly de Souza**
13:00 -14:15 ☺	Lunch Break
14:15 – 16:15	**POSTER SESSION**
16:15 – 16:30 ☺	Coffee break
16:30-17:15	**Unconventional Computing with Novel Materials: Promises and Challenges** **Georgios Ch. Sirakoulis**
17:15-17:35	Mobility and intrinsic performance of silicon-based Nanosheet FETs at 3nm CMOS and beyond **Ankit Dixit**
17:35-17:55	Preliminary numerical study on magnet gate in MOS FD-SOI for quantum and sensor applications **Philippe Galy**
17:55-18:15	Epitaxial p+pn+ vertical short diodes for microbolometers **Romain Kubica**
18:15-18:35	Engineering Thin HZO Ferroelectric Layers: From Material Study to 3D Integration for Vertical Gate-All-Around FeFETs **Konstantinos Moustakas**
18:35	Si/Ge1-xSnx/Si transistors with highly transparent Al contacts **Lukas Wind**
20:00 ☺	Cocktail Reception

Thursday, May 16th

Time	Paper Title
8:30 – 9:00	Registration
09:00-09:45	**Organic neuromorphic electronics for emulating and interfacing biological systems** **Paschalis Gkoupidenis**
9:45-10:05	Temperature-Dependent Electronic Transport in Reconfigurable Transistors based on Ge on SOI and Strained SOI Platforms **Andreas Fuchsberger**
10:05-10:25	Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: transistor performance recovery and back gate bias influence **Carlos Andrés Valdivieso León**
10:25-10:45	Preliminary results on industrial 28nm FD-SOI phase change memory at cryogenic temperature **Philippe Galy**
10:45-11:05	Investigation on the Performance Limits of Dirac-Source FETs **Tommaso Ugolini**
11:05 – 11:20 ☺	Coffee Break
11:20-11:40	Impact of Device Layout on Self-heating Extraction in MOSFETs **Arka Halder**
11:40-12:00	Operation of Junctionless Nanowire Transistors Down to 4.2 Kelvin **Flavio Bergamaschi**
12:00-12:20	Non-Uniform matching performances in mesa-isolated SOI MOSFETs **Pierre Iheritier**
12:20-12:40	Analog Behavior of Forksheet at High Temperatures **Joao Martino**
12:40-13:00	Investigation of DC and Low Frequency Noise Parameters of Junctionless GAA Si VNW pMOSFETs in the Temperature Range from 80 K to 340 K **Abderrahim TAHIAT**
13:00 – 14:15 ☺	Lunch break
14:15-15:50	**Brain-inspired In-memory Computing using Ferroelectric Transistors** **Hussam Amrouch**
15:50-16:10	Novel Y-function methodology parameter estimation from weak to strong inversion operation **Bogdan CRETU**
16:10-16:30	The Dual-Technology FET: nMOS/pTFET in the same device **Joao Martino**
16:30-16:50	TLM-based numerical extraction for CMOS-compatible N+-InGaAs ohmic contacts on 200mm Si substrates **Antoine Lombrez**
16:50 – 17:10	Coffee break
17:20 – 20:30	Excursion to Cape Sounion
21:00	Gala Dinner

Friday, May 17th

Time	Paper Title
9:00-09:45	**Spintronic logic gates and circuits** **Florin Ciubotaru**
9:45-10:05	Effect of Al2O3 on the operation of SiN_x-based MIS RRAMs **Alexandros Mavropoulis**
10:05-10:25	Amorphous TeO2 as P-type Oxide Semiconductor for Electronic Devices **John Robertson**
10:25-10:45	Trap Characterization in Substrates with Buried SiGe Layers for RF **Yiyi Yan**
10:45-11:05	Substrate Crosstalk Characterization for optimized Isolation in FDSOI **Talha Chohan**
11:05 – 11:20 ☺	Coffee Break
11:20-11:40	GaN-on-GaN PiN Diode Performance at Cryogenic Temperatures **Ya-Xun Lin**
11:40-12:00	Low-frequency Noise in Polysilicon Source-Gated Thin-Film Transistor **Qi Chen**
12:00-12:20	DFT study of adsorption density of molecules in 2D materials **Ruben Ortega Lopez**
12:20-12:40	Performance of Pulse-Programmed Memristive Crossbar Array with Bimodally Distributed Stochastic Synaptic Weights **Nadine Dersch**
12:40-13:00	Interface Roughness in Resonant Tunnelling Diodes for Physically Unclonable Functions **Pranav Acharya**
13:00 – 14:15 ☺	Lunch break
14:15-14:35	Influence of multiple MISHEMT conduction channels on analog behavior **Bruno Canales**
14:35-14:55	Optimizing Unconventional Trilayer SOTs for Field-Free Switching **Nils Petter Jørstad**
14:55-15:15	Electron mobility in silicon under high uniaxial strain **Nicolas Roisin**
15:15-15:35	Towards ALD-grown MoS2 devices for CMOS BEOL **Carlos Marquez Gonzalez**
15:35-15:55	Back Bias Effect with Hysteresis in Cryogenic 200 nm SOI MOSFETs **Ryusei RI**
15:55-16:15	Reservoir computing for real-time arrhythmia detection using volatile and non-volatile low power memristors **Dimitris Tsoukalas**
16:15-16:35	Interlayer Exchange Coupling for Enhanced Performance in Spin-Transfer Torque MRAM Devices **Mario Bendra**
16:35-16:55	Quantum Simulations of MoS2 FETs Including Contact Effects **Alfonso Sanchez-Soares**
16:55-17:10	Density Functional Analysis of Voltage Shifts through Oxide Layers in Si- and MoS2-based FETs **Ruyue Cao**
17:10 – 17:30	Conference Closure