

## EuroSOI-ULIS 2024, Poster Session

- 1** TCAD Simulation of GAAFET for Cryogenic Temperature Operation to Achieve Low-Power and High-Performance Applications  
**M-Y Chang, P-C Chen, Y-H Wang, M-H Chiang**

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- 2** A Closed-Form Model for Gauss-Fermi Distribution in Amorphous and Organic Semiconductors  
**N. Dersch, E. Rastegar Pashaki, A. Kloes, G. Darbandy**

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- 3** Boosting the Capacity of Driving the Drain Current of the FinFET by a Simple Changing of the CMOS ICs Manufacturing Process  
**S. Pinillos Gimenez, M. M. Correia**

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- 4** Resistive switching mechanisms in RRAM memory structures based on copper (II) oxide  
**M. Ozga, R. Mroczynski, M. Godlewski, B.j Witkowski**

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- 5** Investigation and Modeling Thermoelectric Performance of Multilayered Sb-rich GeSbTe Phase Change Memory Using Finite Element Method  
**A. Ozturk, H. Cinkaya**

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- 6** Temperature Resilient 1-T FDSOI Neuron for Reliable Neuromorphic Computing  
Rajakumari V, A. Krishna Kumar, **K P Pradhan**

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- 7** TCAD Simulations of Single Event Effects in Quasi-vertical GaN Schottky Barrier Diodes with Guard Rings for Space Applications  
**Y-Xun Lin, D-S Chao, J-H Liang, S. Hall, J. Zhou, I. Mitrovic**

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- 8** Comprehensive study of electrons and spins bound to phosphorus donors in silicon-on-insulator nanostructures  
**F. Taglietti, S. Marzanati, U. Kentsch, R. Quirino, M-J Calderón, B. Koiller, M. Fanciulli**

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- 9** Maintenance-free energy source made of SOI wafers and piezoelectric materials: AlN:Sc and PZT  
J. Zajac, M. Ekwinska, Helena Klos, **D. Szmigiel**, G. Muscalu, S. Dinulescu, C. Moldovan, B. Firtat, A. Anghelescu, G. Sirbu, N. Boice

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- 10** Analog Behavior of V-FET operating in forward and reverse mode  
V.C.P. Silva, A.R. Ribeiro, J.A. Martino, A. Veloso, N. Horiguchi, **P.G.D. Agopian**

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- 11** An Ultra-Low Power VCO for RF Sensing Application  
**R-K Narayanan, D. Stajic, P. Kumar, L. Maurer**

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- 12** Impact of Source-Drain Series Resistance on Carrier Mobility in AlGaN/GaN High Electron Mobility Transistors  
E. Panzo, N. Graziano, E. Simoen, **M. G. C. Andrade**

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- 13** Coupling ab-initio Description and Monte Carlo Simulation to Capture the Transport of Hot Carriers

**M. Ghanem**, R. Sen, J. Sjakste, A. Pilotto, P. Dollfus, J. Saint Martin

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- 14** Recent developments on Thermoelectric devices based on Silicon

**A. Rodriguez-Iglesias**, J. M. Sojo-Gordillo, M. Fernández-Regúlez, I. Martín-Fernández, F. Pérez-Murano, F. Xavier Álvarez, A. F. Lopeandia, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca

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- 15** Monte Carlo Simulation of Thermoelectric Properties of Nanostructures

**M. Ghanem**, Philippe Dollfus, Jerome Saint Martin

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- 16** Stress management in freestanding membranes obtained by ion implantation induced delamination

**L. Benichou**, F. Mazen, T. Salvetat, F. Madeira, F. Rieutord

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- 17** Low power CO<sub>2</sub> detection for sensor integration on FDSOI-CMOS technology for of real-time air quality monitoring

**A. Ghouma**, B. Salem, S. Cavalaglio, J-R. Plaussu, G. Crowin, R. Ben Abbes, S. Monfray, T. Fiorido, M. Bendahan, A. Souifi

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- 18** Machine Learning Augmented TCAD Assessment of Corner Radii in Nanosheet FET

J. Patel, B. Satwik, **N. Bagga**, I. Bais, C. Arora, V. Kumar, A. Dixit, N. Kumar, V. Georgiev, S. Dasgupta

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- 19** Optimization and application of HiPIMS hafnium oxynitride (HfO<sub>x</sub>Ny) thin films in MOS structures

M. Puśniak, W. Gajewski, M. Żelechowski, **R. Mroczynski**

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- 20** Reliability Aspects of Negative-Capacitance Stacked Nanosheet FET Considering Self-Heating Effect

L. Lakkireddy, **S. Srivastava**, Shashidhara M., S. Panwar, J. P. Purohit, L. C. Acharya, A. Acharya

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- 21** Performance Optimization of III-V Homo/Heterojunction Line TFET: Device-Circuit Interaction

**S. Panwar**, K. Kesava, S. Srivatsava, Shashidhara M., S. Rankawat, A. Acharya

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- 22** A Planar Core-Shell Junctionless Transistor Compatible with FD-SOI Technology

**Y. Yan**, W. Song, C. Dou, X. Zhao, B. Li, Y. Xu, S. Cristoloveanu

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- 23** New Insights into Back-Biasing Effects in Advanced FD-SOI MOSFET

**X. Zhang**, Y. Yan, W. Song, C. Dou, X. Zhao, B. Li, Y. Xu, S. Cristoloveanu

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- 24** Nanowire Behavior Under the Influence of Polyoxometalates: A Comparative Study of Depletion and Enhancement Modes

**A. Dixit**, R. Ghosh, J. Jacobs, N. Kumar, L. Vila-Nadal, A. Asenov, D. J. Paul, V. Georgiev

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- 25** Optimizing Peptide Detection Using FET-Based Sensors: Integrating Non-Linearities of Surface Functionalization  
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- 26** A Data Efficient Framework for Higher Dimensional Neural Compact Modeling  
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- 27** Drain Bias Influence on Junctionless Nanowire Transistors Effective Channel Length  
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- 28** Magnetic Spin Hall induced Field-Free Magnetization Switching in SOT-MRAM Devices  
**B. Pruckner**, N. P. Jørstad, W. Goes, S. Selberherr, V. Sverdlov
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- 29** Novel VT1 Reduction Strategies in GGNMOS for Robust ESD Applications  
N. Sarma, A. Yadav, **L. C. Acharya**, R. Singh, S. Dasgupta, A. Bulusu
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- 30** Performance Investigation of 3D Stack Channel Devices  
S. O. Nascimento, **M. G. C. de Andrade**
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- 31** Adaptive Body Biasing Technique based Digital LDO Regulator for Transient Response Improvement  
K. M. Tripathi, M. Pathak, S. Manhas, **A. Bulusu**
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- 32** Temperature Influence on NBTL in Junctionless Nanowire Transistors  
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- 33** Body Bias Assisted Method for Improvement in Performance Parameters of Analog Compute In-Memory Architecture  
**N. Gupta**, L. C. Acharya, M. Dargupally, S. Dasgupta, A. Bulusu
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- 34** Assessing the Performance of Ferroelectric Junctionless FET for NVM  
**A. K. BEHERA**, N. Chauhan, A. Kumar, T. Rampal, S. De, A. Dasgupta, S. Dasgupta, A. Bulusu
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- 35** Silicon-oxide resistive switching memory based on the HSQ layer  
**P. Wisniewski**, A. Mazurak, A. Kadziela, M. Filipiak, B. Stonio, R. B. Beck
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- 36** Study of RRAM devices with PECVD silicon-oxide resistive switching layer  
**I. Lisovyi**, B. Stonio, J. Jasinski, P. Wiśniewski
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- 37** Small Signal PDSOI MOSFET model: Considering Impact Ionization and Self-Heating Effects  
N. P. Singh, S. Banchhor, A. Yadav, A. Goswami, A. Singh, R. Ranjan, S. Dasgupta, **A. Bulusu**
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- 38** A Super low power Frequency Multiplier covering 6 to 9 GHz in 22-nm CMOS-FDSOI Technology  
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- 39** TID aware Efficient Standard Cell Characterization and its Application on the Path level Timing Performance of the Digital Circuits  
**L. C. Acharya, N. Gupta, K. J. Singh, M. Dargupally, N. Mishra, A. Sharma, N. Sarma, A. Yadav, A. Acharya, V. Ramakrishnan, A. Mandal, S. Dasgupta, A. Bulusu**
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- 40** Switching phenomena in CdIn<sub>2</sub>S<sub>4</sub>-based neuromorphic structures  
**J. Zdziebłowski, N. Barreau, P. Zabierowski**
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- 41** Integration of membrane waveguide lasers  
S. Richardson, N. Klokkou, R. Bek, M. Jetter, P. Michler, **V. Apostolopoulos**
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- 42** Assessing the Ion Sensitivity of Si<sub>3</sub>N<sub>4</sub>-based Feedback Field Effect Transistor Using Snap-Back Characteristics  
P. Kumar, **N. Kumar**, A. Dixit, N. Bagga, N. Gandhi, P. N. Kondekar, Md H. R. Ansari, C. P. García, V. Georgiev
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- 43** Simulation of planar CBRAM structures for RF applications  
**E. Tsipas, A. Mavropoulis, E. Stavroulakis, P. Dimitrakis, G. Ch. Sirakoulis**